REMARKS

Claims 1-16 and 23-30 are pending in the present application. Replacement claims 2-8, 10-12 and 14-16 have been presented herewith. Also, claims 23-30 have been presented herewith.

Priority Under 35 U.S.C. 119

Enclosed is a copy of a Claim of Priority letter dated September 27, 2002, submitted along with Japanese priority application 2000-104733. Also enclosed is a dated, stamped postcard receipt provided as evidence that the Claim of Priority letter has been received by the U.S. Patent Office. **The Examiner is respectfully requested to acknowledge receipt of the certified copy of the priority document, and to confirm on the record that the Claim for Priority is complete.**

Information Disclosure Statement

Enclosed is a copy of an Information Disclosure Statement and citation form filed along with the present application on April 5, 2001. Also enclosed is a dated, stamped postcard receipt as evidence that the Information Disclosure Statement was received by the U.S. Patent Office. **The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement, and to confirm on the record that the corresponding documents have been considered and will be cited of record in the present application.**

Claim Rejections-35 U.S.C. 112

Claims 1-16 have been rejected under 35 U.S.C. 112, first paragraph, as allegedly containing subject matter not described in the specification in such a way as to reasonably convey that the inventors had possession of the claimed invention. This rejection is respectfully traversed for the following reasons.

The Examiner has noted that the Brodsky et al. reference (U.S. Patent No. 6,323,130) teaches that cobalt disilicide has a lower resistance than cobalt monosilicide, and that the Yamanaka et al. reference (U.S. Patent No. 5,915,197) teaches an alternative method to form cobalt disilicide to avoid metal-agglomerated silicides which have higher sheet resistances. Applicants do not necessarily disagree with the above noted positions as taken by the Examiner in view of the Brodsky et al. and Yamanaka et al. references.

However, Applicants respectfully emphasize that as described beginning on page 8, line 5 of the present application, when the **contact specific resistance between refractory metal and silicon** becomes less than 1×10^{-7} Ω-cm^2, the parasitic resistance of the transistor does not increase and the drive current of the transistor thus is not reduced. Particularly, the present application is concerned with contact specific resistance **between** refractory metal and silicon. In contrast, the Brodsky et al. and Yamanaka et al. references as considered by the Examiner are concerned with

resistance of a cobalt disilicide layer, not a contact specific resistance between a refractory metal and silicon as in the present application.

Accordingly, Applicants respectfully submit that one of ordinary skill would readily understand the meaning of a metallic silicide layer comprised of CoSiz in which a ratio of cobalt to silicon is 1 to z ($1<z<2$). Applicants respectfully submit that claims 1-16 are in compliance with 35 U.S.C. 112, first paragraph, and that Applicants clearly had possession of the claimed invention. Accordingly, the Examiner is respectfully requested to withdraw this rejection for at least the above reasons.

Conclusion

Since the above noted rejection under 35 U.S.C. 112 should be withdrawn at least in view of the above noted comments, and since no prior art rejections are currently outstanding, Applicants respectfully submit that claims 1-16 should now be in condition for allowance. Applicants also respectfully submit that dependent claims 23-30 as presented herewith should also be allowable for at least the same reasons.

Applicants also respectfully submit that the claims have been amended merely to improve form, rather than to further distinguish over any of the prior art of record. This should be especially clear since the claims have not been rejected based upon prior art. Accordingly, the above noted amendments should not be construed as narrowing scope within the meaning of *Festo*.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicants hereby petition for an extension of three (3) months to June 19, 2003, for the period in which to file a response to the outstanding Office Action. The required fee of $930.00 is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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Enclosures: Version with Marked-Up Changes
Copy of Claim of Priority Letter
Copy of postcard receipt
Copy of Information Disclosure Statement
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VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Specification:

Page 1, lines 4-6:

The present application [claiming] claims priority under 35 U.S.C. 119 to Japanese Application No. 2000-104733 filed on April 6, 2000, which is hereby incorporated by reference in its [entirely] entirety for all purposes.

Page 1, lines 10-14:

The present invention relates to a field effect transistor (FET) which is formed in a silicon layer located on an insulating film, or a silicon on insulator (SOI) substrate. The SOI substrate has an insulating film and a thin silicon layer formed over a conductive substrate [is] used as the conventional substrate to form the FET. The present invention also relates [, and] to a method of manufacturing such a field effect transistor.

Page 4, lines 13-15:

According to the present invention, [a] the field effect transistor is capable of restraining the reduction of the drive current thereof. The transistor of the present invention can be formed in a microscopic size.

Page 6, lines 12-15:

Fig. 1 is a cross-sectional view describing a field effect transistor according to a first preferred embodiment, [for detail, typicality] showing in detail a fully depleted SOI-FET formed on an SOI substrate. The SOI-FET is formed in a thin silicon film (SOI layer) which is formed on an insulating film of the SOI substrate.

Page 11, lines 11-15:

In fact, it will be expected that the contact specific resistance [go] would be further [reduce] reduced, by considering the accumulation resistance Rac, the spreading resistance Rsp and the sheet resistance Rsh-s in the above formula. The contact specific resistance between the cobalt silicide (CoSix) and the silicon of the first preferred embodiment is far smaller than $1x10^{-7}\ \Omega\text{-cm}^2$ introduced in the above second thesis.

Page 11, line 16 through to page 12, line 7:

Fig. 4 is an explanation diagram showing the drain voltage dependence of a threshold voltage for the fully depleted SOI-FET. In Fig. 4, the SOI-FET is the N type MOS transistor, as well as Fig. 3(a) and Fig. 3(b). The drain voltage of the conventional SOI-FET is shown as a mark of "X" and that of the first preferred embodiment is shown as a mark of "●". When a substrate floating effect, such as a parasitic bipolar effect occurs in the fully depleted SOI-FET, the drain voltage will rise up. Fig. 4 shows that a reduction of a threshold voltage of the conventional SOI-FET is remarkable, as a drain

voltage rises up. However, the reduction of the threshold voltage of the SOI-FET of the first preferred embodiment is [loose] minimal. In other words, a leakage current of the SOI-FET can be cut down.

Page 12, lines 8-12:

According to the first preferred embodiment of the present invention, a field effect transistor capable of restraining the reduction of the drive current of the SOI-FET is provided. Further, the SOI-FET of the first preferred embodiment enables [to form] formation of microscopic devices. Additionally, since the SOI-FET of the first preferred embodiment can precisely reduce the leakage current, the SOI-FET is useful as a low-power transistor.

Page 13, lines 8-16:

The source and the drain regions include the highly doped silicon layers 18a and 18b and metallic silicide layers 19a and 19b, respectively. The metallic silicide layers 19a and 19b are composed of refractory metal and silicon. An amount of refractory metal contained in the metallic silicide layers 19a and 19b is more than that of silicon. In the second embodiment as well as the first embodiment, the metallic silicide layers 19a and 19b are comprised of a CoSiz layer having a ratio of cobalt to silicon that is one to z ($1<z<2$). The [CoSix] CoSiz layers 19a and 19b are formed by the conventional silicide process. [For] In more detail, the source region and the drain

region [expect] except under the sidewalls 7a and 7b are changed into the cobalt silicide layers 19a and 19b.

Page 13, line 17 through to page 14, line 4:

The CoSiz layers 19a and 19b respectively have a thickness which is equal to or more than 80% thickness of from top surfaces of the CoSiz layers 19a and 19b to bottom surfaces of the SOI layer 3. In other words, portions 21a and 21b of the highly doped silicon layers 18a and 18b respectively extend between bottom surfaces of the [CoSix] CoSiz layers 19a and 19b and a top surface of the insulating layer 2.

Page 14, lines 5-7:

[A] If a conventional $CoSi_2$ layer is used as the metallic silicide layer[. The], the conventional $CoSi_2$ layer [is] would be formed so as to have a thickness of the $CoSi_2$ layer less than 80% thickness of from top surfaces of the $CoSi_2$ to bottom surfaces of the SOI layer.

Page 14, lines 8-10:

On the other hand, 1993 IEEE, pp. IEDM 93-723 ~ 726-IEDM 93, "[OPTIMIZATIN] OPTIMIZATION OF SERIES RESISTANCE IN SUB-0.2 m SOI MOSFETs" (hereinafter a third thesis), reports [as follows.] the following concerning a conventional $CoSi_2$ layer:

Page 15, line 9 through to page 16, line 2:

A method of manufacturing the field effect transistor described in the third preferred embodiment, will be shown hereinafter referring to Fig. 5(a) – Fig. 5(c). In Fig. 5(a), the SOI-FET is formed on an SOI substrate, which comprises a silicon substrate 51, an insulating film 52, and an SOI layer 53. Field oxide films 56a and 56b and heavily doped impurity layers 58a and 58b are formed in the SOI layer 53 by using a conventional process. A channel region is defined between the pair of highly doped silicon layers 58a and 58b. A gate electrode 55 is formed on a gate oxide film 54 and located on the channel region. Cobalt (Co) film 60 is formed on the gate electrode 55 and highly doped silicon layers 58a and 58b. The cobalt film 60 is a refractory metal film for forming a metallic silicide layer. A titanium (Ti) film 61 or a titanium nitride (TiN) film 61 are formed on the cobalt film 60 as an antioxidant film 61 when a following heat treatment.

Page 17, line 12 through to page 18, line 1:

According to the present invention, a field effect transistor capable of restraining the reduction of the current drive capacity of the transistor is provided. Also, the transistor as provided enables [to form] formation of microscopic devices including the SOI-FET described above. Since the transistor of the present invention can precisely reduce the leakage current, a low-power transistor can be provided. Additionally, as a small amount of silicon remains under the metallic silicide layers, a field effect transistor having a low resistance and a stable metallic silicide layer can be provided.

Additions/Deletions to the Claims:

2. (Amended) The field effect transistor according to claim 1, wherein said field effect transistor has a depletion layer which expands to [the] bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

3. (Amended) A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on [an] the insulating layer, wherein the semiconductor layer includes the channel region therein;

a pair of impurity layers formed in regions [where] which are respectively in contact with the channel region in the source region and the drain region; and

a pair of cobalt silicide layers respectively formed in the source region and the drain region, wherein the pair of cobalt silicide layers are respectively in contact with the pair of impurity layers, wherein bottom surfaces of the pair of cobalt silicide layers extend to bottom surfaces of the semiconductor layer;

wherein the cobalt silicide layers are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to α ($1<\alpha<2$).

4. (Amended) The field effect transistor according to claim 3, wherein said field effect transistor has a depletion layer which expands to [the] bottom surfaces of the

source region and the drain region when a voltage is supplied to the gate electrode thereof.

5. (Twice Amended) A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on the insulating layer, wherein the semiconductor layer includes the channel region defined by the source region and the drain region;

a pair of impurity layers formed into regions which are respectively in contact with the channel region in the source region and the drain region; and

a pair of metallic silicide layers respectively formed in the source region and the drain region, wherein the pair of metallic silicide layers are respectively in contact with the pair of impurity layers, wherein the pair of metallic silicide layers have a thickness which is equal to or more than 80% thickness of from [the] an upper surface of the metallic silicide layers to [the] a bottom surface of the semiconductor layer;

wherein the metallic silicide layers are composed of refractory metal and silicon, and

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following inequality:

$(X / Y) > (X0 / Y0)$.

6. (Amended) The field effect transistor according to claim 5, wherein said field effect transistor has a depletion layer which expands to [the] bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

7. (Amended) A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on [an] the insulating layer, wherein the semiconductor layer includes the channel region therein;

a pair of impurity layers formed in regions [where] which are respectively in contact with the channel region in the source region and the drain region; and

a pair of cobalt silicide layers respectively formed in the source region and the drain region, wherein the pair of cobalt silicide layers are respectively in contact with the pair of impurity layers, wherein the pair of cobalt silicide layers has a thickness which is equal to or more than 80% thickness of from [the] an upper surface of the cobalt silicide layers to [the] a bottom surface of the semiconductor layer;

wherein the cobalt silicide layers are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to α ($1<\alpha<2$).

8. (Amended) The field effect transistor according to claim 7, wherein said field effect transistor has a depletion layer which expands to [the] bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

10. (Amended) The field effect transistor according to claim 9, wherein said field effect transistor has a depletion layer which expands to [the] bottom surfaces of the source region and the drain region when a voltage is supplied to [the] a gate electrode thereof.

11. (Amended) A field effect transistor formed in a semiconductor layer located on an insulating layer, the field effect transistor having a source region and a drain region formed in the semiconductor layer, comprising:

the source region including a first impurity layer and a first cobalt silicide layer, wherein the first impurity layer and the first cobalt silicide layer are formed so as to reach the insulating layer through the semiconductor layer; and

the drain region including a second impurity layer and a second cobalt silicide layer, wherein the second impurity layer and the second cobalt silicide layer are formed so as to reach the insulating layer through the semiconductor layer;

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is defined by the first impurity [region] layer and the second impurity layer, and

wherein the first cobalt silicide layer and the second cobalt silicide layer are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to α ($1<\alpha<2$).

12. (Amended) The field effect transistor according to claim 11, wherein said field effect transistor has a depletion layer which expands to [the] bottom surfaces of the source region and the drain region when a voltage is supplied to [the] a gate electrode thereof.

14. (Amended) The field effect transistor according to claim 13, wherein said field effect transistor has a depletion layer which expands to [the] bottom surfaces of the source region and the drain region when a voltage is supplied to [the] a gate electrode thereof.

15. (Amended) A field effect transistor formed in a semiconductor layer located on an insulating layer, the field effect transistor having a source region and a drain region formed in the semiconductor layer, comprising:

the source region including a first impurity layer and a first cobalt silicide layer, wherein the first cobalt silicide layer [have] has a thickness which is equal to or more than 80% thickness of from [the] an upper surface of the first cobalt silicide layer to [the] a bottom surface of the semiconductor layer; and

the drain region including a second impurity layer and a second cobalt silicide layer, wherein the second cobalt silicide layer [have] has a thickness which is equal to or more than 80% thickness of from [the] an upper surface of the second cobalt silicide layer to [the] a bottom surface of the semiconductor layer;

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is defined by the first impurity [region] layer and the second impurity layer, and

wherein the first cobalt silicide layer and the second cobalt silicide layer are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to α ($1<\alpha<2$).

16. (Amended) The field effect transistor according to claim 15, wherein said field effect transistor has a depletion layer which expands to [the] bottom surfaces of the source region and the drain region when a voltage is supplied to [the] a gate electrode thereof.